

REMARKS

Claim 36 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is overcome by the cancellation of claim 36.

The Examiner has indicated that claims 4-7 and 34 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. This objection is overcome by the amendment of independent claims 1 and 17.

Claims 1-3, 8-12, 15 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Shin* (U.S. Pat. No. 6,804,724) in view of *Bergstrom et al.* (U.S. 5,307,379). Claims 13 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Shin/Bergstrom* as applied to claim 1 above, and further in view of National Semiconductor, "An Overview of LVDS Technology", Application Note 971, July 1998 ("*National*"). Claims 17, 18, 21-33, 35 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Bergstrom et al.* in view of *National*. Claims 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Bergstrom/National* as applied to claim 17 above, and further in view of *Shin*. Applicants traverse these rejections on the grounds that these references are defective in establishing a *prima facie* case of obviousness.

Independent claims 1, 17 and 35 each include:

1. A computer system comprising:
 - a first processor;
 - a transmission line coupled to the first processor;

a monitor including a receiver input gate coupled to the transmission line;
changing circuitry coupled to the transmission line and to the receiver input gate and capable of changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of the receiver input gate, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the change is made;

a synchronization processor coupled to the receiver input gate;

monitoring circuitry coupled to the synchronization processor and capable of monitoring an output of the synchronization processor and detecting irregularly timed synchronization processor output signals; and

wherein the changing circuitry is further capable of changing at least one of the pedestal voltage level and the signal threshold voltage level when the monitoring circuitry detects irregularly timed output signals.

17. A method of reducing an effect of signal distortion from reflection on a transmission line, comprising:

changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of a receiver input gate coupled to the transmission line, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the changing, and such that the effect of signal distortion from reflection on the transmission line is reduced;

detecting the effect of signal distortion from reflection on the transmission line caused by a substantial equality of the pedestal voltage level and the signal threshold voltage level; and

the detecting including monitoring an output of the synchronization processor for irregularly timed output signals by comparison to phasing of an output of a video amplifier.

35. An apparatus for reducing an effect of signal distortion from reflection on a transmission line, comprising:
- means for changing at least one of a pedestal voltage level on the transmission line and a signal threshold voltage level of a receiver input gate coupled to the transmission line, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the changing, and such that the effect of signal distortion from reflection on the transmission line is reduced;
 - means for detecting the effect of signal distortion from reflection on the transmission line caused by a substantial equality of the pedestal voltage level and the signal threshold voltage level; and
 - the means for detecting including monitoring an output of the synchronization processor for irregularly timed output signals by comparison to phasing of an output of a video amplifier.

As the PTO recognizes in MPEP §2142:

...The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Examiner does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of nonobviousness.....the Examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made....The Examiner must put aside knowledge of the Applicant's disclosure, refrain from using hindsight, and consider the subject matter claimed 'as a whole.'"

The references fail to teach or suggest the claimed subject matter.

Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. §103 rejection because the cited references fail to teach or even

suggest the desirability of the combination. Moreover, the references fail to provide any incentive or motivation supporting the desirability of the combination.

The MPEP §2143.01 provides:

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Therefore, the Examiner's combination arises solely from hindsight based on the invention without any showing of suggestion, incentive or motivation in either reference for the combination.

Thus, the Examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met.

The Federal Circuit has, on many occasions, held that there was no basis for combining references to support a 35 U.S.C. §103 rejection. For example, in *In re Geiger*, the court stated in holding that the PTO "failed to establish a *prima facie* case of obviousness":

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. *ACS Hospital Systems, Inc. v. Monteffiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

The Federal Circuit has also repeatedly warned against using the Applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teachings

in the prior art. See e.g., *Grain Processing Corp. v. American Maize-Products*, 840 F.2d 902, 907, 5 USPQ2d 1798, 1792 (Fed. Cir. 1989).

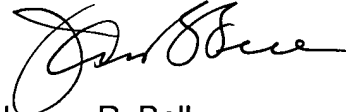
More recently, the Federal Circuit found motivation absent in *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). In this case, the court concluded that the board had “reversibly erred in determining that one of [ordinary] skill in the art would have been motivated to combine these references in a manner that rendered the claimed invention [to have been] obvious.” The court noted that to “prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness.” The court further noted that there were three possible sources for such motivation, namely “(1) the nature of the problem to be solved; (2) the teachings of the prior art; and (3) the knowledge of persons of ordinary skill in the art.” Here, according to the court, the board had relied simply upon “the high level of skill in the art to provide the necessary motivation,” without explaining what specific understanding or technological principle within the knowledge of one of ordinary skill in the art would have suggested the combination. Notably, the court wrote: “If such a rote invocation could suffice to supply a motivation to combine, the more sophisticated scientific fields would rarely, if ever, experience a patentable technical advance.”

Therefore, independent claims 1, 17 and 35, and the claims dependent therefrom are submitted to be allowable.

In view of the above, it is respectfully submitted that claims 1-3, 5-17, 19-30, 32 and 35 are in condition for allowance. Accordingly, an early Notice of Allowance is courteously solicited.

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Respectfully submitted,



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